Development of a Compact 28-GHz Software-Defined Phased Array for a City-Scale Wireless Research Testbed

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***Abstract*— This paper reports the development of a compact and highly programmable 28-GHz phased array subsystem that is currently being integrated in a city-scale testbed for advanced wireless research and experimentation. The subsystem hardware consists of a 28-GHz 64-element state-of-the-art dual-polarized phased array antenna module (PAAM), low-noise DC-DC power regulators with a single 12-V input, current sensors and an ADC for real-time supply monitoring, a PLL for LO (5 GHz) generation, IF (3 GHz)/LO splitters, IF/LO baluns, and programmable switches. All of these components are integrated in a compact (10"×5.75") PCB which also supports the direct plug-in of a commercial-off-the-shelf FPGA system-on-module (SoM). The IF switches and splitters couple the PAAM to 20 IF ports that enable a rich set of MIMO configurations, including up to 8 simultaneous 16-element independent beams in each TX/RX mode. The FPGA and associated software enable the configuration of all subsystem features from a high-level application program interface (API), facilitating MIMO millimeter-wave wireless experiments. 28-GHz channel sounding measurements using the phased array subsystem coupled with software-defined radios is presented as a testbed-level experiment example.**

***Keywords*— phased array, antenna arrays, beam-steering, millimeter wave communication, wireless communication, 5G mobile communication, MIMO, software-defined networking.**

I. Introduction

The maturation of emerging wireless communication technologies such as millimeter-wave, distributed MIMO, and dynamic spectrum access, and their linkage to new applications, requires experimentation at scale and in realistic environments. In this context, several city-scale programmable testbeds are being implemented globally to support advanced wireless research and development for academia and industry [1], [2], [3]. Among them, the COSMOS testbed is currently being deployed in West Harlem (New York City) as part of the NSF Platforms for Advanced Wireless Research (PAWR) program by Rutgers University, Columbia University, and NYU in partnership with New York City (NYC), City College of New York (CCNY), IBM, University of Arizona, and Silicon Harlem [4], [5], [6].

This paper reports the development of a compact software-defined 28-GHz phased array subsystem which is one of the key radio components in the COSMOS testbed to enable ultra-high bandwidth and ultra-low latency wireless applications. Fig. 1 illustrates three key layers of the COSMOS testbed architecture that support millimeter-wave experiments

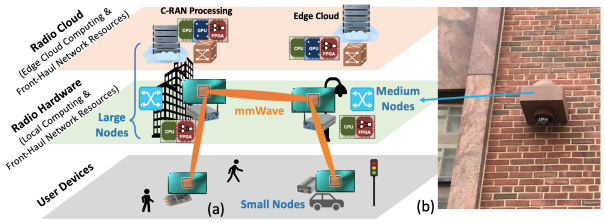

Fig. 1. (a) COSMOS testbed's multi-layered computing architecture; (b) appearance of a wall-mounted medium node on the street level.

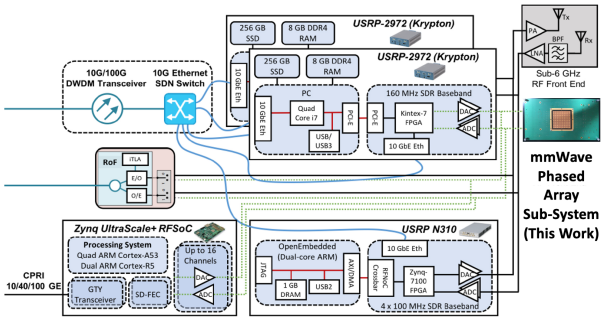

Fig. 2. Block diagram of a medium node in COSMOS testbed.

and that enable multiple levels of programmability and control from user devices to the cloud. The testbed will include wall-mounted or lightpole-mounted medium nodes that integrate sub-6 GHz (already deployed) and additional 28-GHz millimeter-wave phased array subsystems integrated with software-defined radios (e.g., USRP-2974 and USRP-N310 shown in Fig. 2). Fig. 3 presents a block diagram of the software-defined phased array subsystem illustrating the vertical integration of hardware and software components to enable the control of beamforming and radio functions from a high-level API that can be utilized for test-bed level experiments.

In this paper, Section II presents the hardware development of the 28-GHz phased array antenna module (PAAM) subsystem board including architecture, key features, and design layout that are based on extensive test vehicle characterization. Section III describes the overall software control architecture that optimizes beam-forming performance. Finally, a real-time 28-GHz channel sounding demonstration is shown as a testbed experiment example.

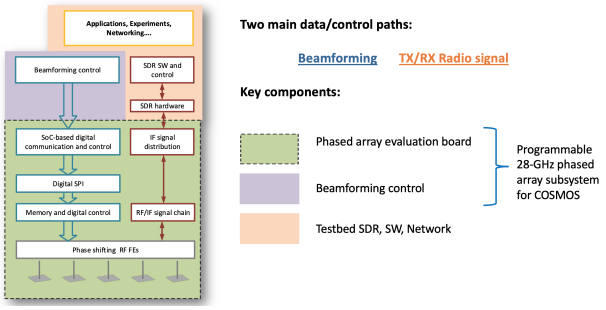

Fig. 3. 28-GHz phased array subsystem architecture and its integration with testbed software

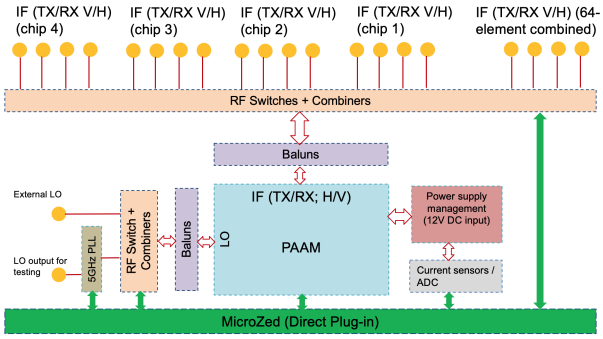

Fig. 4. 28-GHz phased array antenna module (PAAM) subsystem board architecture.

II. Hardware Development of 28-GHz Phased Array Subsystem Board

Fig. 4 illustrates a block diagram of the 28-GHz PAAM subsystem board, which represents a significant extension beyond the earlier hardware for software-defined phased array demonstration [9]. The board integrates a 28-GHz dual-polarized 64-antenna-element PAAM (Fig. 5-(a)) [7], low-noise DC-DC power converters with a single 12V input, a built-in PLL for 5-GHz LO generation, current sensors with ADC, as well as IF/LO baluns, RF splitters, and programmable switches. The board has a 3-GHz single-ended IF interface to baseband via SMT connectors. The RF switches-based programmability of the power combiner tree enables the

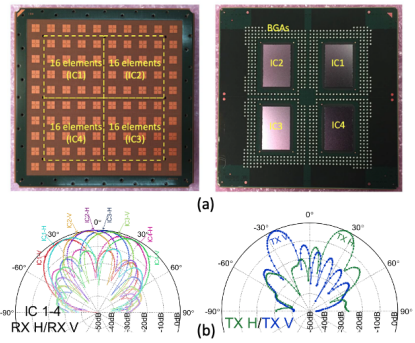

Fig. 5. (a) 28-GHz phased array antenna module (PAAM) [7]; (b) Flexible beam-forming support: 16-element beams and 64-element beams in H and V polarization [8].

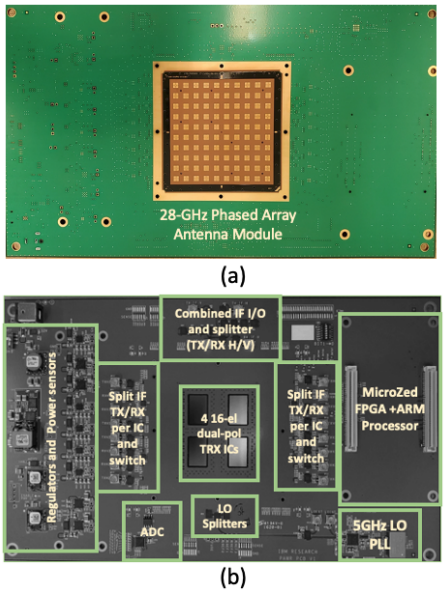

Fig. 6. (a) Front view of the 28-GHz PAAM board; (b) back view with an illustration of function blocks.

PAAM to form either two 64-element (one H-pol, one V-pol) beams or eight 16-element (four H-pol, four V-pol) beams in both TX and RX modes (Fig. 5-(b)) [8]. The switch configurations for TX and RX modes in each polarization are independent. An additional switch is provided to support bypass of the on-board PLL with an externally provided LO. The board also supports direct plug-in of a low-cost MicroZed FPGA [10] for digital control and programming.

Two different test vehicle boards were designed, fabricated, and characterized to validate and demonstrate the required functionality. Key components for power supplies, frequency reference, PLL/LO, RF balun, splitter, switch, current sensors, and ADC were down-selected based on passive and active testing results.

Fig. 6 presents detailed photographs of the final assembled PAAM board, which is 5.75" by 10" in size. As can be observed, the only component placed on the top surface of the board is the PAAM; this approach enables close placement of the radome with respect to the PAAM. On the bottom side of the board, all surface mount components are placed and all IF connectors for TX/RX beam-forming ports are available. The back surfaces of the ICs assembled on the PAAM are accessible through rectangular openings in the PCB to enable direct thermal contact of those ICs with a heatsink. On the right side, the board features a multi-pin digital connector for the direct placement of an FPGA card that is required for PAAM configuration and the control of all other board functions, including LO initialization, switch configuration, and ADC readout of DC current values.

A key aspect of the PAAM board layout was the routing of the 3-GHz IF signal and the associated switches and power combiners. The routing starts with the differential IF ports at the PAAM-board interface. The signals are routed to baluns

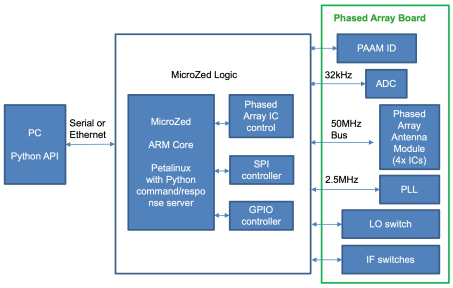

Fig. 7. 28-GHz PAAM board software and firmware control architecture.

(for conversion to single-ended signaling) and then to switches that select whether the signals go directly to SMP connectors (providing access to 16-element beams) for external access or to power combiners (to form 64-element beams). An important challenge that was overcome in this design is that all of the IF signal routing from the PAAM interface to the SMP connectors should be symmetrical. Any IF routing mismatch introduced prior to the connection to the combiners creates a phase shift that has to be compensated at RF. The symmetrical routing obviates the need for any calibration at the board level, simplifying board use.

III. Software Control and Functional Demonstration

There are three sections in the PAAM board control architecture as shown in Fig. 7. First, at the top of the stack, a set of Python scripts can be executed from the testbed servers that are also connected to the software-defined radios. This section of the software features an API that enables the execution of high-level PAAM control commands and that can be called from testbed-level experimental scripts. Second, the Python scripts hosted on the control server communicate with the MicroZed FPGA mounted on the PAAM board via an ethernet or a serial connection. On the receive side, another set of Python scripts are executed using the ARM processor core in the FPGA. Third, the low-level communication protocols with the PAAM board components are implemented in the MicroZed FPGA. These firmware components are responsible for control of the PAAM itself (TX/RX mode of operation, number of active phased array elements, beam-forming control, etc.), as well as control of the supporting board components, e.g., the PLL for LO generation, an ADC for DC current monitoring, IF switches to configure the number of simultaneous beams that the board can provide, a switch for bypassing on-board LO, as well as a unique ID for each board.

This PAAM control software/firmware architecture and the partitioning of functions between the server processors and FPGA enables flexibility for testbed-level experiments that can be executed by a remote user during the reservation window, while preserving fast execution speed and reduced latency for low-level PAAM configuration functions.

The clock frequency for the PAAM control is approximately 50 MHz, which is made possible by the use of short, well-matched traces on the PCB. The PAAM control firmware, in combination with the Python scripts, enable high-speed PAAM control for beam-forming (e.g., <1 milli-second for RFIC initialization, beam-forming, and beam-steering).

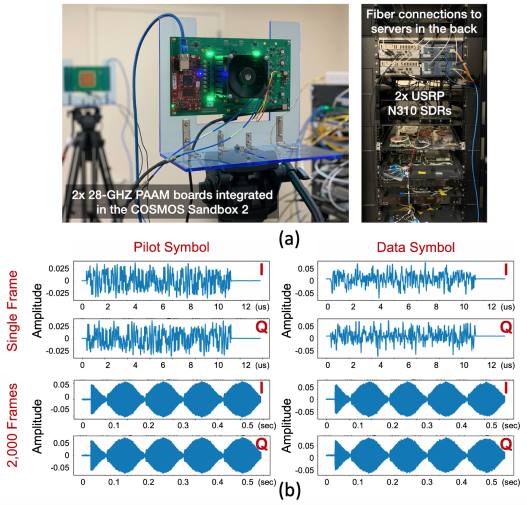

Fig. 8. A 28-GHz SISO channel sounding demonstration: (a) two PAAM boards integrated with USRP N310 SDRs and compute servers; (b) pilot and data I/Q waveforms with fast beam switching capability.

Fig. 8 shows a recent indoor real-time single-input and single-output (SISO) link demonstration using two 28-GHz PAAM boards, one emulating a base station and one a client. A single-IC configuration was applied in TX and RX mode with 8 H-polarization front-end elements activated. The PAAM boards were integrated with two separate USRP N310 software-defined radios that ran 62.5-MHz bandwidth OFDM signals. The resulting pilot and data I/Q signal waveforms for channel sounding and communications, respectively, were successfully computed and demonstrated. As an example of simultaneous beamsteering and data capture operations, during the 2000-frame long sequence shown in Fig. 8 (b), the RX beam is continuously steered from -30 to +30 degrees in steps of 1 degree (each step approx. each 2ms). This beamsteering sequence is repeated 4.5 times. As it can be observed, the received amplitude from the pilot symbols changes in proportion to the beam direction.

IV. Conclusion

A compact phased array subsystem board with 64 dual-polarized antennas has been developed for COSMOS testbed deployment to enable city-scale directional communication experiments in the 28-GHz band. Supporting firmwave and control software enable ample flexibility for controlling beam-forming for millimeter-wave wireless experiments, including the ability to control: (i) the number of ICs and number of elements in each IC to be activated; (ii) beam-forming modes (e.g., TX/RX beam-forming in H/V polarization); and (iii) beam-steering directions and beam-forming weights (amplitude and phase).

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